GERA-2113

SPACE SHUTTLE SYNTHETIC APERTURE RADAR-FINAL REPORT

CONTRACT NO. JPL-953053
CONTRACT WORK ORDER NO. 10

SUBMITTED TO

CALIFORNIA INSTITUTE OF TECHNOLOGY
JET PROPULSION LABORATORY
4800 OAK GROVE DRIVE
PASADENA, CALIFORNIA 91103

GERA-2113

12 AUGUST 1975

GOODYEAR AEROSPACE CORPORATION
ARIZONA DIVISION • • • LITCHFIELD PARK, ARIZONA

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ABSTRACT

This report presents the results of a feasibility study performed to investigate a digital signal processor for real-time operation with a synthetic aperture radar system aboard the Space Shuttle. This report includes pertinent digital processing theory, a description of the proposed system, and size, weight, power, scheduling, and development estimates.

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SECTION I - INTRODUCTION

This report presents the results of a study program in which the feasibility of developing a digital signal processor to be an integral part of the Space Shuttle Synthetic Aperture Radar (SAR) was determined. The study examined the geometries and beam tracking corrections associated with an orbital radar mapping system, the technologies available for implementing the processor, the architecture of the processor, tradeoffs which can influence the design, and such factors as the size, weight, and power consumption of a representative design. A program schedule and cost have also been derived. Costs for the processor configuration derived here have been estimated using components which semiconductor manufacturers' representatives have forecast to be readily available by 1977. Obviously, dramatic breakthroughs (or setbacks) such as the semiconductor industry has continually experienced, could influence these estimates. However, digital signal processors for synthetic aperture radar systems having complexities comparable to the Space Shuttle Synthetic Radar task are presently being developed. Therefore, it is felt that advances in the semiconductor field will not affect the performance achievable with a digital signal processor, but could impact the hardware by which it is implemented and the cost of the development.

Table I, which was supplied by Jet Propulsion Laboratory, presents the radar characteristics for which this processor has been configured. Table II defines the variables used in this report.

The processor configuration described in this report is capable of processing L-band and X-band radar data at a real-time rate. Although the range dimension processing for the two radar frequencies is virtually identical, the azimuth dimension hardware required for the L-band processing exceeds that necessary for X-band by more than a factor of six. As the L-band operations dominate the processing to such a degree, this mode will be used for all design within this report, and the X-band will be considered as a fallout from the design.

TABLE I - RADAR CHARACTERISTICS (ALTITUDE = 185 KM)

Parameters	L-band			X-band		
Frequency (GHz)	1.3			8.33		
Wavelength (m)	0.23			0.036		
Quantization (bits)	6			6		
Azimuth looks (image)	4 or 8			4 or 8		
Range looks (image)	1, 2, 4			1, 2, 4		
Presum number	1			1		
Transmitted pulse width (μs)	23.0			21.0		
Range ambiguity (dB)	20			20		
Azimuth ambiguity (dB)	22.5			22.5		
Image dynamic range (dB)	50			50		
Image grayscale resolution (dB)	1			1		
Spatial resolution (m) nominal	25, 50			25, 50		
Antenna azimuth dimension (m)	12			12		
Bandwidth* (MHz) (I and Q each)	17.38			17.38		
Receive time (μs)	329			329		
Off-nadir angle (deg)	25	38	50	25	38	50
Antenna elevation dimension (m)	0.65	1.55	2.2	0.12	0.24	0.36
PRF	1860	1615	1900	1850	1615	1900
Swath width (km)	100	78.1	62.6	100	78.1	62.6
Range compression ratio	400	400	400	365	365	365
Length of azimuth channels (m)	1188	1414	1704	186	221	267
Range to swath center (km)	205	244	294	205	244	294

*Assumes 26 percent broadening of main response of the compressed pulse.

TABLE II - VARIABLES AND ABBREVIATIONS

ACF = azimuth compression filter

A/D = analog-to-digital

α = orbit inclination with respect to equator

β = antenna beamwidth

B = bandwidth

C = speed of light

δR_g = ground range resolution

δR_s = slant range resolution

ϵ = beamwidth required for one synthetic aperture

f_d = doppler frequency

γ = compliment of the doppler cone angle

h = spacecraft altitude

I = in-phase (real) data component

K = sidelobe weighting factor

λ = radar wavelength

L_{syn} = synthetic aperture length

N = number of bits in a digital word

Φ = signal phase

ϕ = off-nadir angle

PRF = pulse repetition frequency

TABLE II - VARIABLES AND ABBREVIATIONS (CONT)

ψ = azimuth pointing angle

Q = quadrature (imaginary) data component

RAM = random access memory

RCF = range compression filter

ROM = read-only memory

R_g = ground range

R_s = slant range

ρ = radius of earth = 6367.7 km

τ = transmitter pulse length

θ_g = angle between slant range vector and surface of earth

V_E = tangential velocity of earth at equator = 463.07 m/s

V_{REL} = velocity of spacecraft relative to earth

W_a = azimuth resolution

W_r = range resolution

Twelve-bit complex words (6-bit I and Q) have been selected for the azimuth compression memory. Twelve-bit complex samples are large enough to preserve the input dynamic range without having small signal suppression or spurious target generation effects result. Because range compression and azimuth filtering have been performed prior to this storage, the dominant noise source will be the rounding of the samples to six bits. Quantization noise has a uniform distribution; thus, it is readily shown that the dynamic range of the signals stored in this memory (peak signal-to-rms quantization noise) is 40.8 dB.

Specifications require that 50 dB of dynamic range be available for both frequencies at the processor output. The increase in dynamic range when azimuth compression is performed is

$$\text{dynamic range increase} = 10 \log \frac{K^2 \lambda R_s}{2W_a^2} \text{ dB} \quad . \tag{1}$$

Equation (1) exceeds 10 dB for all operating modes. An additional 3-dB increase in dynamic range will also be obtained when the four azimuth looks are summed. Thus, greater than 50-dB dynamic range will be available at the processor output.

All memories in this report are semiconductor devices. Although discs, drums, etc., were considered, it appears that in the time frame of this design semiconductors will provide the most cost-effective storage for synthetic aperture processing.

Finally, this report describes a processor capable of real-time operation for all radar data at one frequency and polarization. Cost savings are possible by designing the equipment to process the data at a fraction of real time, to process only a fraction of the range swath per pass of the data, or to process only one or two azimuth looks per pass of the data. The viability of such tradeoffs will be determined by user requirements, however, and will not be considered further in this report.

SECTION II - SIGNAL PROCESSOR DESIGN

1. AZIMUTH MEMORY REQUIREMENTS

The majority of the storage in the digital signal processor is that required to perform azimuth compression and to combine azimuth looks. From Table I, it is seen that the longest synthetic aperture to be processed is 1704 meters, which occurs when the off-nadir angle is 50 degrees at L-band. In the digital signal processor, the azimuth spacing will be reduced to the minimum possible, i.e., one complex sample per the reciprocal of the required bandwidth. Because of the 26-percent excess spatial bandwidth, this becomes 19.84 meters per sample for 25-meter resolution. Dividing the synthetic aperture length by this sample spacing results in a maximum of 86 samples per look to be processed. For 38 degrees off-nadir, 72 samples are necessary, and for 25 degrees off-nadir, 60 samples are necessary. The number of range samples in each PRF is the product of the A/D converter rate and the receiver time, less the number of samples in an uncompressed range pulse; hence, 5353 range gates will be required to store each PRF after range compression. In summary, the memory size is seen to be dictated by the off-nadir angle requiring the maximum storage, which is the 50-degree case, for which 460,358 complex word storage locations are required for each look. Because each complex word is 12 bits, and because four looks are to be processed, the azimuth compression memory will require 22.1 megabits of storage.

In addition to the azimuth compression storage, it is necessary to provide a delay of three synthetic aperture lengths to store processed data until corresponding looks at the same target are available. Because detected data are being stored, a sample spacing of one-half the desired resolution should be maintained. As the data have been converted to ground range, the 50-degree off-nadir angle mode will require the largest amount of storage, a total of 2.454 megawords. Nine-bit words will be adequate for this task.

2. COMPENSATION FOR ANTENNA POSITION

The radar antenna is not stabilized. Thus, to properly focus the data, corrections must be made in the processor to compensate for the antenna's deviations about the desired pointing angle. Compensation for shuttle roll (which will introduce dopplers caused by the separation of the antenna from the spacecraft) and center of gravity acceleration and for orbit characteristics will require data to be input to the processor from external sources.

The actual off-nadir angle of the antenna beam can be estimated by measuring the average return power as a function of range. The effects of the earth's rotation require relatively straightforward calculations which can be performed by a minicomputer.

The azimuth pointing angle of the antenna must be determined by a clutterlock because it can deviate by as much as 2 degrees from the yaw angle of the shuttle. Because this exceeds the 3-dB antenna beamwidth by a factor of 4 in L-band and a factor of 26 at X-band, and the PRF is adequate for sampling only the doppler within the antenna beam, the number of beamwidths of displacement must be calculated. In addition, pitch rotation of the antenna (which will cause the azimuth and elevation patterns to interchange) will add a linearly changing doppler offset as a function of the range to the clutterlock signal.

A straightforward technique for resolving the ambiguity and determining the pitch and yaw angles requires that the clutterlock be range gated. Because the intersection of a cone of constant doppler with the earth (for a flat, nonrotating earth approximation) is a hyperbola, the doppler frequency in the center of the beam will change as a function of range (except when the antenna is pointed perpendicular to the plane of the orbit). Figure 1 illustrates the intersection of the pointing angle vector to a line of constant doppler (isodop).

The cone angle of the isodop which the azimuth yaw vector intersects was calculated by a computer program. Analysis of the computer data verified that sufficient curvature exists to resolve the antenna pointing ambiguity. To initialize the clutterlock, a portion

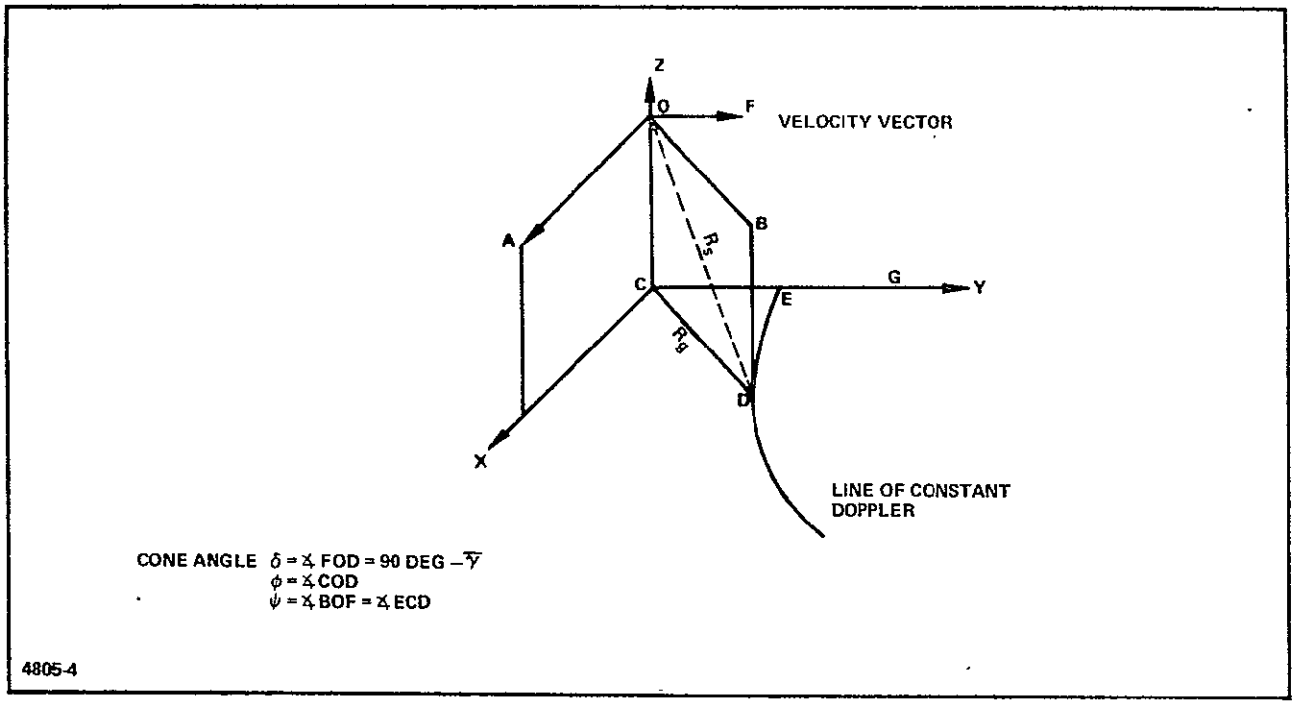


Figure 1 - Cone Angle Geometry

of the data tape equivalent to a few synthetic apertures may be recorded in an auxiliary storage and "run backward;" i.e., PRF number N, N - 1, . . . , 1. The final values in the clutterlock thus become the initial conditions when the data tape is processed.

After the pitch and yaw angles have been resolved, the clutterlock will continue to track the motion of the beam. It would appear to be beneficial to process the L-band data first, because of the lower number of ambiguities from which the pointing angle must be determined. The clutterlock signal from this processing could then be stored and used to provide additional aid for the X-band signals.

The doppler frequency at the center of the antenna beam as a function of γ, the complement of the cone angle, is given by

$$f_d = \frac{2V}{\lambda} \cos \gamma \quad , \tag{2}$$

where

$$\gamma = \arccos(\sin\psi \sin\phi) \quad .$$

Hence, for a given value of ψ, the doppler in the center of the antenna beam across the range swath is given by

$$\Delta f_d = \frac{2V}{\lambda} \sin\psi \left[\sin\phi_{max} - \sin\phi_{min}\right] \quad . \tag{3}$$

Table III presents the doppler frequency for various values of ϕ and ψ. The pitch angle has been assumed to be zero, although similar tables may be readily derived for nonzero values.

TABLE III - TABULATED DOPPLER FREQUENCIES (L-BAND)

Yaw angle, ψ (deg)	0.5	1.0	2.5	5.0	7.5	10.0
Off-nadir angle, ϕ (deg)						
15	152.7	306.6	768.3	1530.5	2291.4	3048.4
20	202.4	404.9	1012.1	2021.6	3028.3	4028.4
25	249.8	500.7	1250.0	2498.4	3741.2	4978.1
30	295.9	591.9	1479.6	2956.2	4426.6	5889.0
35	339.7	679.5	1697.4	3379.5	5078.4	6755.3
40	380.0	761.2	1902.1	3800.3	5690.9	7571.1
45	419.1	836.9	2092.4	4179.7	6260.4	8328.2
50	453.4	906.8	2254.7	4528.2	6782.4	9022.1
55	485.3	969.5	2423.9	4842.3	7252.2	9648.2
60	512.6	1025.1	2562.3	5119.7	7667.5	10199.7

3. COMPENSATION FOR ROTATION OF THE EARTH

To properly clutterlock and focus synthetic aperture radar data, a correction must be made for the rotational velocity of the earth (463.07 m/s at the equator). Figure 2 illustrates the extremes of relative velocity as a function of the orbit altitude for various orbit inclinations.

In addition, target motion will be caused by rotation of the earth. A target at near range will have a lower relative radial velocity component than a target at far range because of the slant range geometry. Thus, a correction signal must be generated which varies as a function of range. This is illustrated for a polar orbit in Figure 3. Over the period of a synthetic aperture at L-band at a 25-degree off-nadir angle, a target at far range will change in slant range by approximately 30 meters more than one at near range. As this exceeds eight range gates (slant range), a range slippage correction which varies as a function of range will also be required. The variation in range slippage is illustrated in Figure 3.

Note that corrections similar to the above must also be made if the spacecraft deviates from a circular orbit.

4. RANGE WALK AND RANGE CURVATURE

The definitions and geometries of range walk and range curvature are presented in Figure 4. Range curvature, which is proportional to the amount of quadratic phase error measured about a best linear fit for a synthetic aperture, is given by

$$\text{range curvature} = \frac{\left(L_{syn}\right)^2}{8R_s} \quad ,$$

where L_{syn} is the synthetic aperture length, and R_s is the slant range to the target.

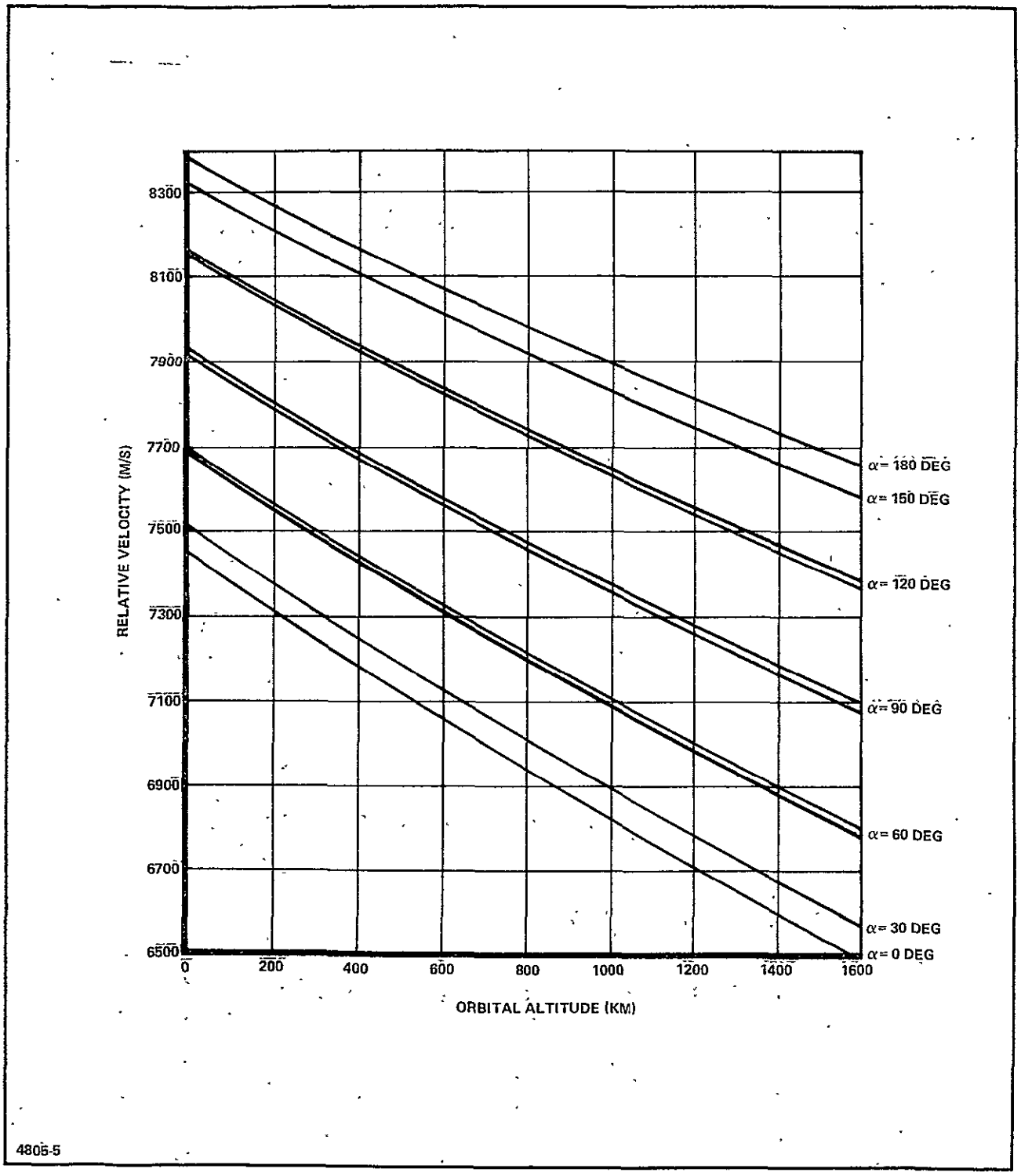
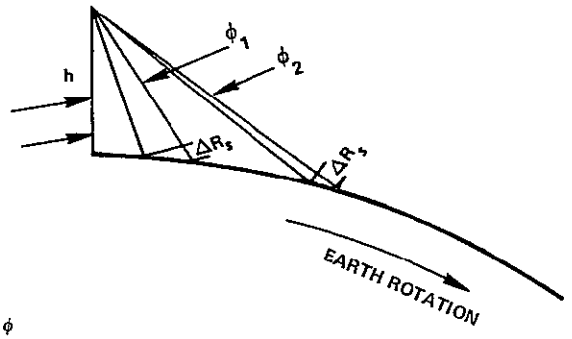


Figure 2 - Relative Velocity versus Orbital Altitude



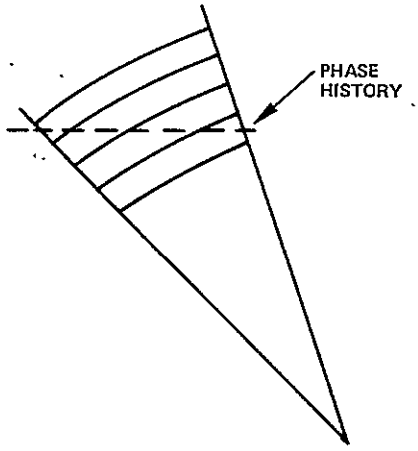
$\Delta V_g = \Delta V_s \text{ SINE } \phi$

FOR L-BAND MAPPING AT EQUATOR				
OFF-NADIR ANGLE (DEG)	SYNTHETIC APERTURE TIME (S)	NEAR RANGE TARGET VELOCITY (M/S)	FAR RANGE TARGET VELOCITY (M/S)	Δ RANGE SLIPPAGE PER SYNTHETIC APERTURE (M)
25	0.149	60.44	262.28	30.1
38	0.186	269.30	332.90	11.8
50	0.223	348.33	378.35	6.7

VARIABLE RANGE SLIPPAGE IS REQUIRED TO COMPENSATE FOR THE EARTH'S ROTATION

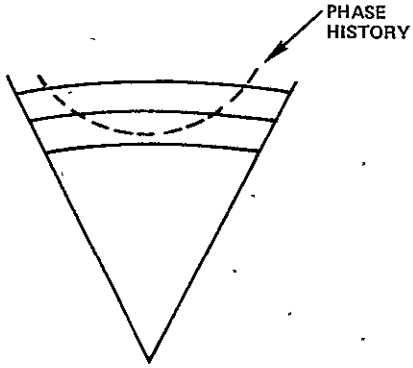
4805-6

Figure 3 - Variation in Range Slippage



RANGE WALK

RANGE WALK IS CAUSED BY THE PHASE HISTORY LYING IN MORE THAN ONE RANGE GATE DUE TO THE ANTENNA BEAM OR LOOK ANGLE SKEW. RANGE WALK CORRECTION IS A LINEAR PHASE ADJUSTMENT.



RANGE CURVATURE

RANGE CURVATURE EFFECTS OCCUR WHEN THE VARIATION OF A SECTION OF A PARABOLIC PHASE HISTORY ABOUT A STRAIGHT LINE APPROXIMATION APPROACHES OR EXCEEDS A RANGE RESOLVABLE ELEMENT.

4805-7

Figure 4 - Range Walk and Range Curvature Definitions

From the values in Table I, the maximum range curvature occurs at L-band for a 50-degree off-nadir angle and equals 1.23 meters. The slant range samples are spaced by 8.63 meters. Analysis has shown that the effect of this 14-percent displacement upon resolution and sidelobes is virtually negligible.

The correction for range walk will be performed as two distinct operations which will be referred to as fine and coarse range slippage. Fine range slippage is the resampling of the data such that a given return remains at the same position relative to the new data samples. Coarse range slippage advances (or retards) the data by an integer number of range gates. These operations are illustrated in Figure 5.

For a squinted beam, the per sample range change, ΔR, is given by the equation

$$\Delta R = \frac{V \sin \psi \sin \Phi}{PRF} \quad . \tag{4}$$

Note that ψ will differ for each of the four azimuth looks, and that both ψ and Φ change with range.

5. REQUIRED NUMBER OF AZIMUTH REFERENCE FUNCTIONS

It has been shown that 5353 range samples are to be processed for each of the four looks. The generation of 21,412 different reference functions would require an enormous amount of hardware. Fortunately, this is not necessary.

Analysis has shown that satisfactory results may be achieved if the azimuth phase history and azimuth compression reference functions are mismatched by no more than 45-degree peak phase error. Therefore, as the phase, Φ, is given by

$$\Phi = \frac{4\pi R_s}{\lambda} \approx \Phi_o + \frac{2\pi X^2}{\lambda R_{s0}} \quad , \tag{5}$$

where R_{s0} is the slant range to the center of the azimuth phase history, the peak phase error occurs when

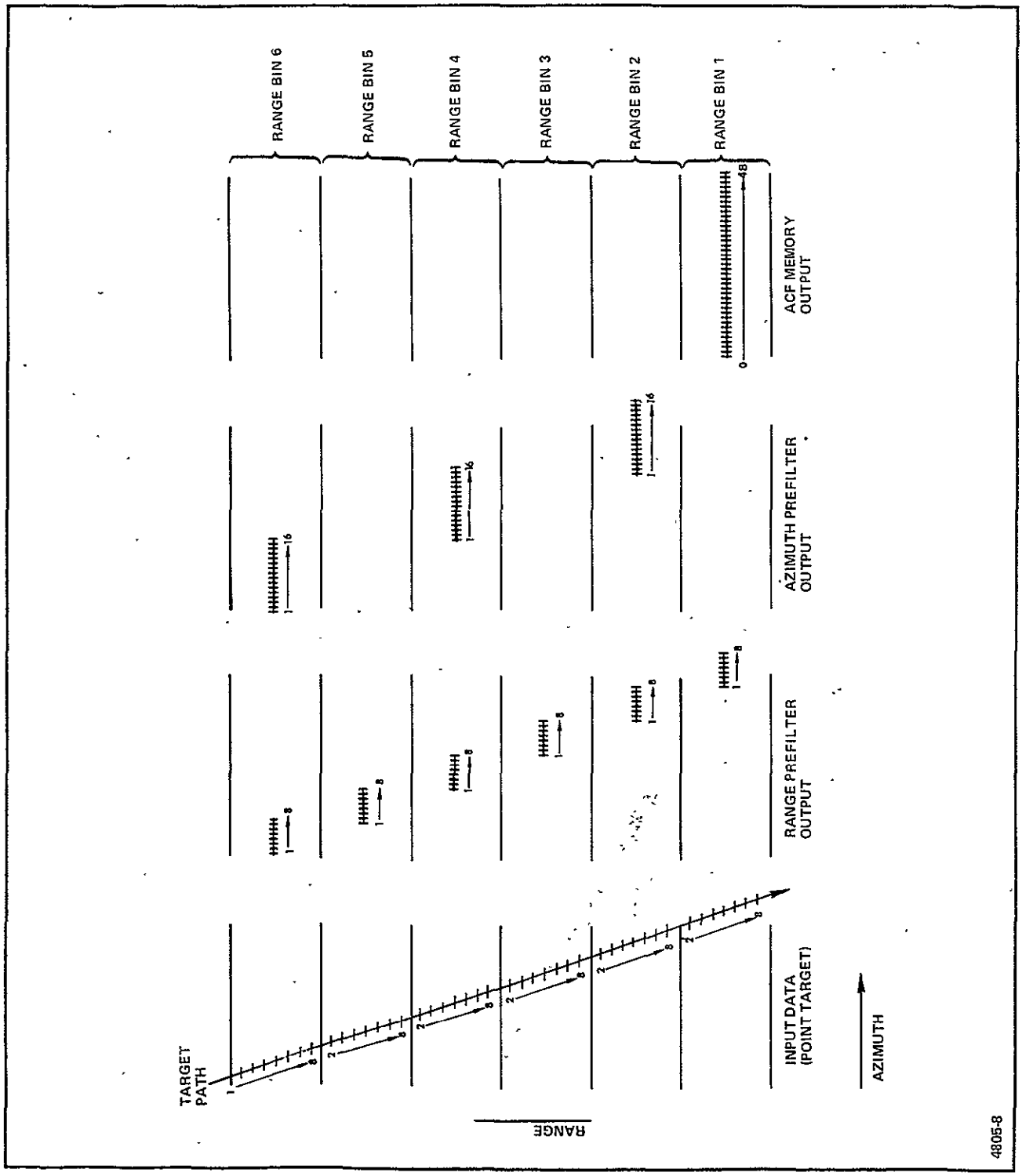


Figure 5 - Range Slippage Correction

$$X = \frac{1}{2}L_{syn} = \frac{1.26\lambda R_{s0}}{4W_a} \quad . \tag{6}$$

Then,

$$\Delta\Phi = \frac{2\pi X^2}{\lambda R_{s0}}\left(\frac{\Delta R_s}{2}\right) = \frac{(1.26)^2\lambda\pi}{16W_A^2}\Delta R_s = \frac{\pi}{4} \quad , \tag{7}$$

$$\Delta R_s = \frac{4W_A^2}{(1.26)^2\lambda} \quad ,$$

where ΔR_s is the slant range interval for which one azimuth reference function may be utilized.

For the L-band processing, ΔR_s = 6800 meters. Hence, fewer than 10 reference functions will suffice for processing each azimuth look.

6. SLANT RANGE TO GROUND RANGE CONVERSION

Slant range to ground range conversion is an interpolation process which will transform evenly spaced data points from a straight line into evenly spaced data points on a circle. This geometry is illustrated in Figure 6. This process will be performed after azimuth compression to minimize storage requirements.

The ground and slant range samples have the approximate relationship

$$\delta R_g = \delta R_s \sec\theta_g \quad . \tag{8}$$

The angle θ_g is calculated from the relationship

$$\frac{\sin(90 \text{ deg} + \theta_g)}{h + \rho} = \frac{\sin(\phi)}{\rho} \quad . \tag{9}$$

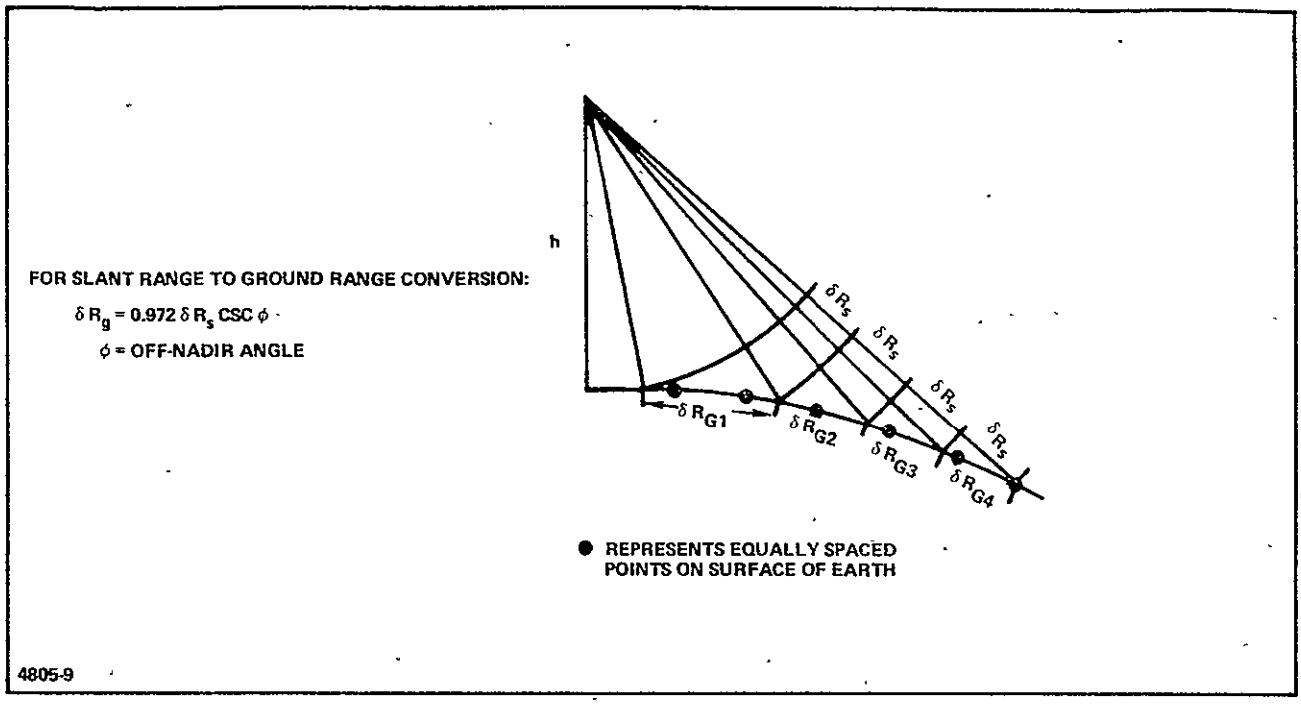


Figure 6 - Slant Range to Ground Range Conversion

For a 185-km orbit, θ_g is given by

$$\theta_g = \cos^{-1}(1.029 \sin\phi) \quad . \tag{10}$$

Thus,

$$\delta R_g = 0.972\ R_s \operatorname{cosec}\phi \quad ; \tag{11}$$

where the instantaneous value of ϕ is given by

$$\phi = \cos^{-1}\left[\frac{R_s^2 + h^2 + 2\rho h}{2R_s(h + \rho)}\right] \quad . \tag{12}$$

The slant range to ground range conversion will resample the data to produce ground range samples spaced by 12.5 meters prior to detection. Data at near range will have proportionately poorer resolution. Data at far range, for which the ground range resolution will be better than that specified, will be effectively filtered to 25-meter resolution with one and a fraction range looks when the resampling process is performed.

7. PROCESSOR OUTPUT SAMPLING RATE

The spectra of the processor output before and after detection are presented in Figure 7. As can be seen, the detection process doubles the signal bandwidth; thus, it is desirable to double the output sampling rate in both the range and azimuth dimensions to preserve the processed resolution.

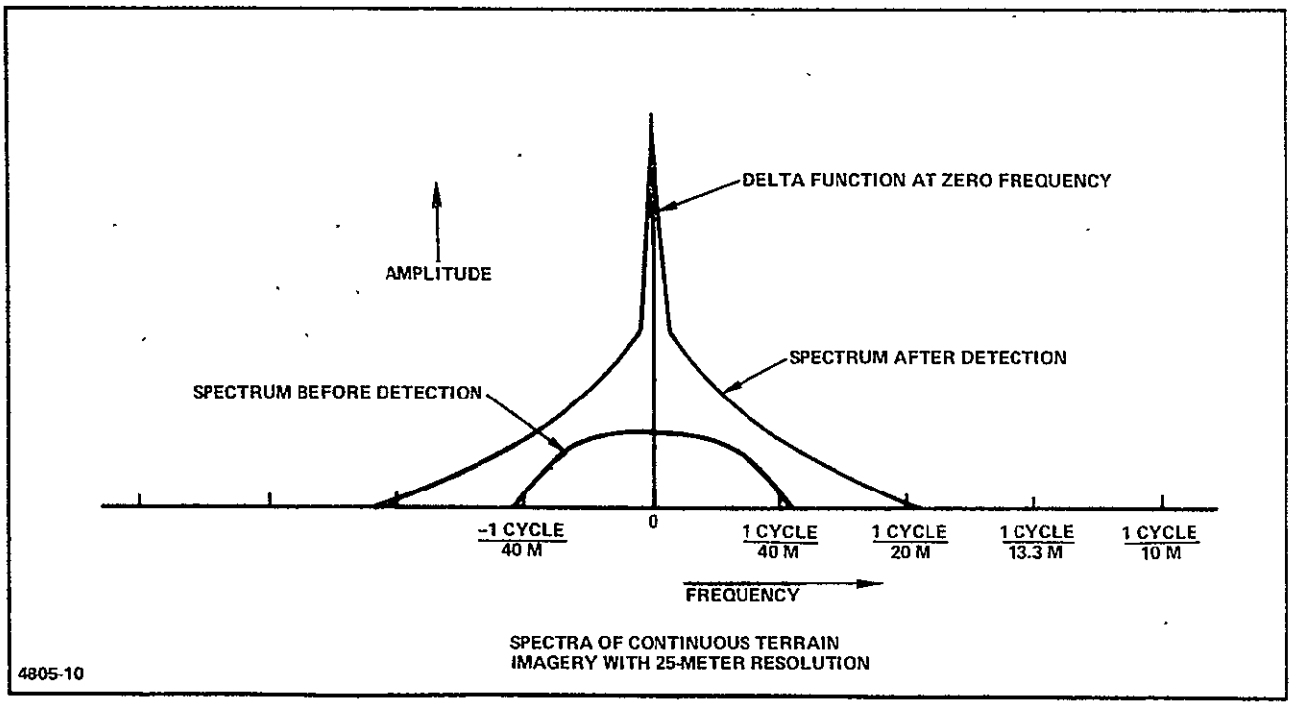


Figure 7 - Spectra of Continuous Terrain Imagery with 25-Meter Resolution

Although it would be possible to reduce the size of the 22.9 megabit azimuth look storage if larger sampling spaces were used, the resultant savings would have little effect on the overall system cost, and the mean resolution of the system would be reduced. Thus, 12.5 meter sample spacing is recommended for the data after detection.

8. AZIMUTH MULTIPLE LOOKS

When processing synthetic aperture radar data, all or part of the doppler bandwidth may be processed for resolution. If the total bandwidth is used for resolution, the resultant processed signal contains all the information about the target which can be obtained (assuming the system is linear). Therefore, a multiple-look system can never gather more information about any target than a one-look system having the same bandwidth (when the system is linear).

If the bandwidth is divided into sections, several signals may be derived from the total bandwidth, each of which when processed yields proportionately less resolution. When the target is composed of random features, the pieces of the total bandwidth will be statistically identical but uncorrelated. When the target is regular on a scale larger than the maximum resolution length, the pieces of the bandwidth will be correlated and nonstatistical in nature. Thus, combining the multiple looks will result in a better image than any look by itself.

Two methods for the production of multiple looks, illustrated in Figure 8, are:

1. Filtering to form multiple bandwidth sections, with each section processed coherently and the results detected and summed
2. Processing for ultimate resolution and low-pass filtering detected outputs to the desired resolution.

Studies have shown that these two methods of producing multiple looks are virtually identical in terms of the quality of the resulting image.

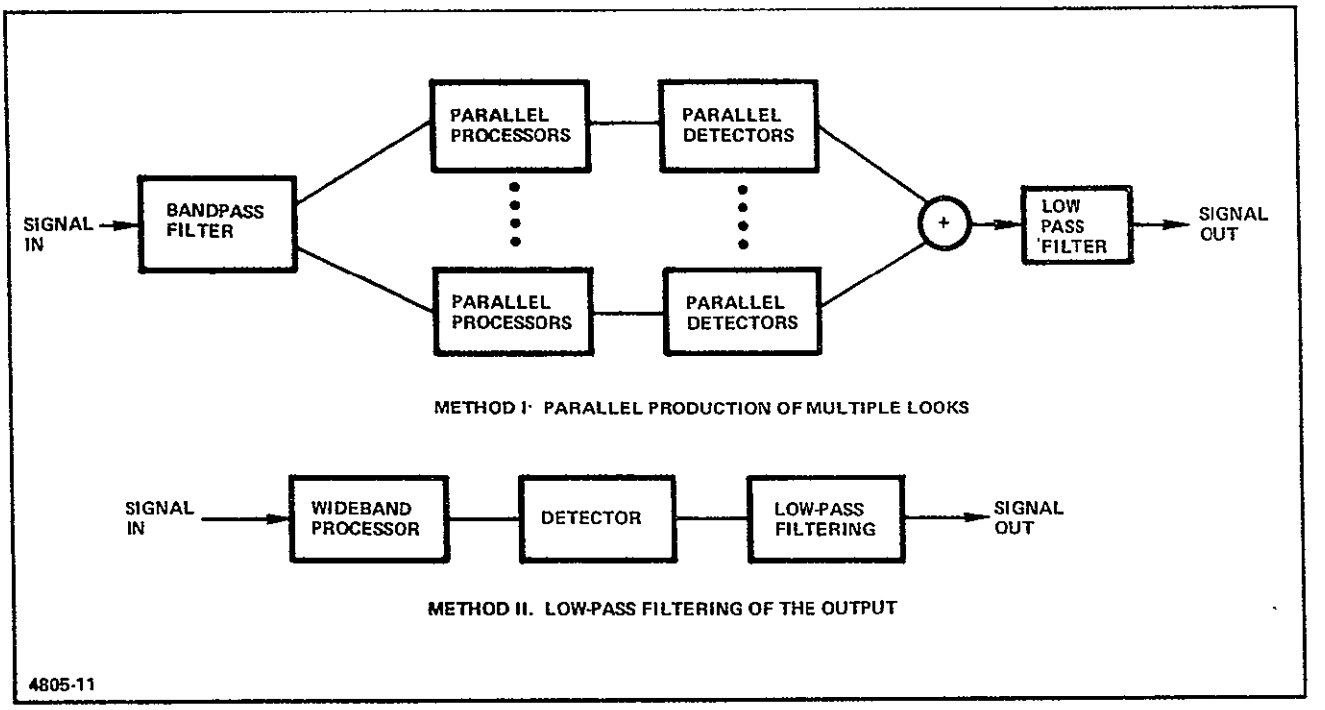


Figure 8 - Two Methods Used for Producing Multiple Looks

For the processor to be discussed in Section IV, Method 1 will be employed for the azimuth four-look mode, because this method requires the least amount of storage to be utilized in the azimuth compression filter. Method 2 will be employed when more than four azimuth looks and more than one range look are desired (with a corresponding decrease in resolution). Implementation of Method 2 requires very little additional hardware to implement when configured with the four-look processor.

SECTION III - PROCESSOR SIGNAL FLOW

Figure 9 is included to show the sequence of the operations required to process the data and the flow of the image and navigation data throughout the processor. The hardware and algorithms to be used to perform these operations will be detailed in Section IV. Although some of the operations listed will be performed simultaneously, while the performance of others may be distributed throughout many subunits, the general order and location in which they are shown is correct. It is hoped that this diagram will assist the reader in comprehending the overall operation of the digital signal processor.

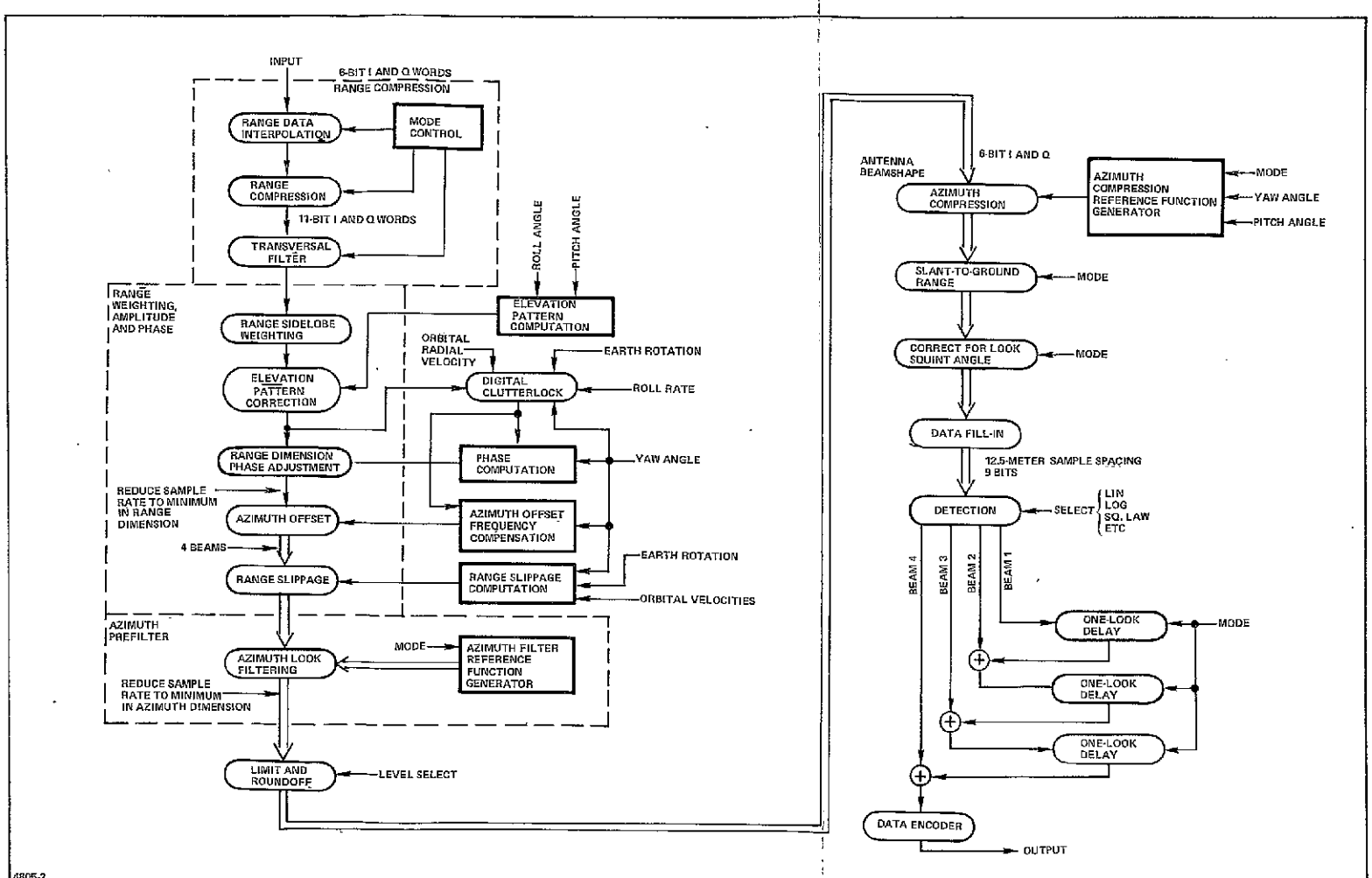


Figure 9 - Space Shuttle SAR Processing Flow

SECTION IV - PROCESSOR DESCRIPTION

1. INTRODUCTION

In this section, a digital signal processor capable of producing imagery with the desired resolution and number of looks at a real-time rate will be configured. The algorithms and the order in which they are implemented have been shown by experience to produce adequate performance and can be implemented with hardware designs balanced in speed, size, power, maintainability, and cost. The processor is designed to handle data recorded on tape with a 100-percent duty cycle.

The system has been designed about the parameters detailed in Sections I and II. Growth of the system for higher orbit altitudes is discussed at the end of this section. The sizing has been performed about components (primarily memory elements) which have high probabilities of being available within the next two to three years.

Figure 10 is an overall block diagram of the digital signal processor.

2. RANGE COMPRESSION FILTER

The range compression filtering is the first operation to be performed by the digital signal processor. Although compression requirements increased the dynamic range, and a correspondingly larger word size is required for storage of each sample, factors such as phase corrections and clutterlock accuracies make collapsing of the range pulse desirable at this point.

An iterative range compression algorithm has been selected for this analysis. As illustrated in Figure 11(A), the parabolic phase of a chirp signal is approximated by a piecewise linear approximation in the range compression filter (RCF), with the resulting phase error shown in Figure 11(B). Each straight line segment can be implemented by an iterative filter having linear phase. Noise buildup in the filter is avoided by allowing only 0, 90, or 180 degree phase shifts within the loops. This choice results in a very small

number of complex multiplications (four if $B\tau = 400$) being required for each output data point. This is because all time samples of the matched filter function for $B\tau = 400$ have phases divisible by 18 degrees, and with proper presumming only multiplications by the sines of 18 degrees, 36 degrees, 54 degrees, and 72 degrees are necessary (0 degrees and 90 degrees being trivial operations).

Range compression ratios with the property described above have square roots which are integer divisible by four. The algorithm can be employed with a pulse having any dispersion ratio smaller than that of the filter by simply adjusting the sampling rate of the digitized signal to match the frequency versus time slope of the filter. If the signal has a time-bandwidth product, $B\tau$ and the filter $B'\tau'$, then the sampling rate increase is a factor of $\left((B'\tau')/B\tau\right)^{1/2}$. This can be accomplished by either an increase in the A/D conversion rate of this factor or by an interpolation filter (which has been included in the sizing of this processor).

If the transmitted waveform were a "stairstep" chirp signal, it and the RCF would be matched. For a linear chirp signal, the phase error illustrated in Figure 11(B) occurs. The results of this mismatch are "paired-echo" images of the collapsed pulse. Thus, a transversal filter is necessary to generate a delayed, phase shifted, and attenuated signal which is added to the output to remove these sidelobes. This has also been included in the estimate.

The range pulse compression algorithm described in this section has been shown to require an interpolation circuit to match the FM rate of the signal and the RCF, and a transversal filter to remove the sidelobes caused by phase mismatch. The transversal filter may be eliminated if the transmitted waveform were a stairstep chirp instead of a linear chirp. The interpolation network may be eliminated either by the choice of $B\tau$ products whose square roots are exactly divisible by four (e.g., 64, 144, 256, 400, 596, etc.), or by the approximately 5-percent increase in the A/D conversion rate. These devices have been included in the estimate, however, to provide the user with virtually any compression ratio desired (assuming in this design it is less than 400).

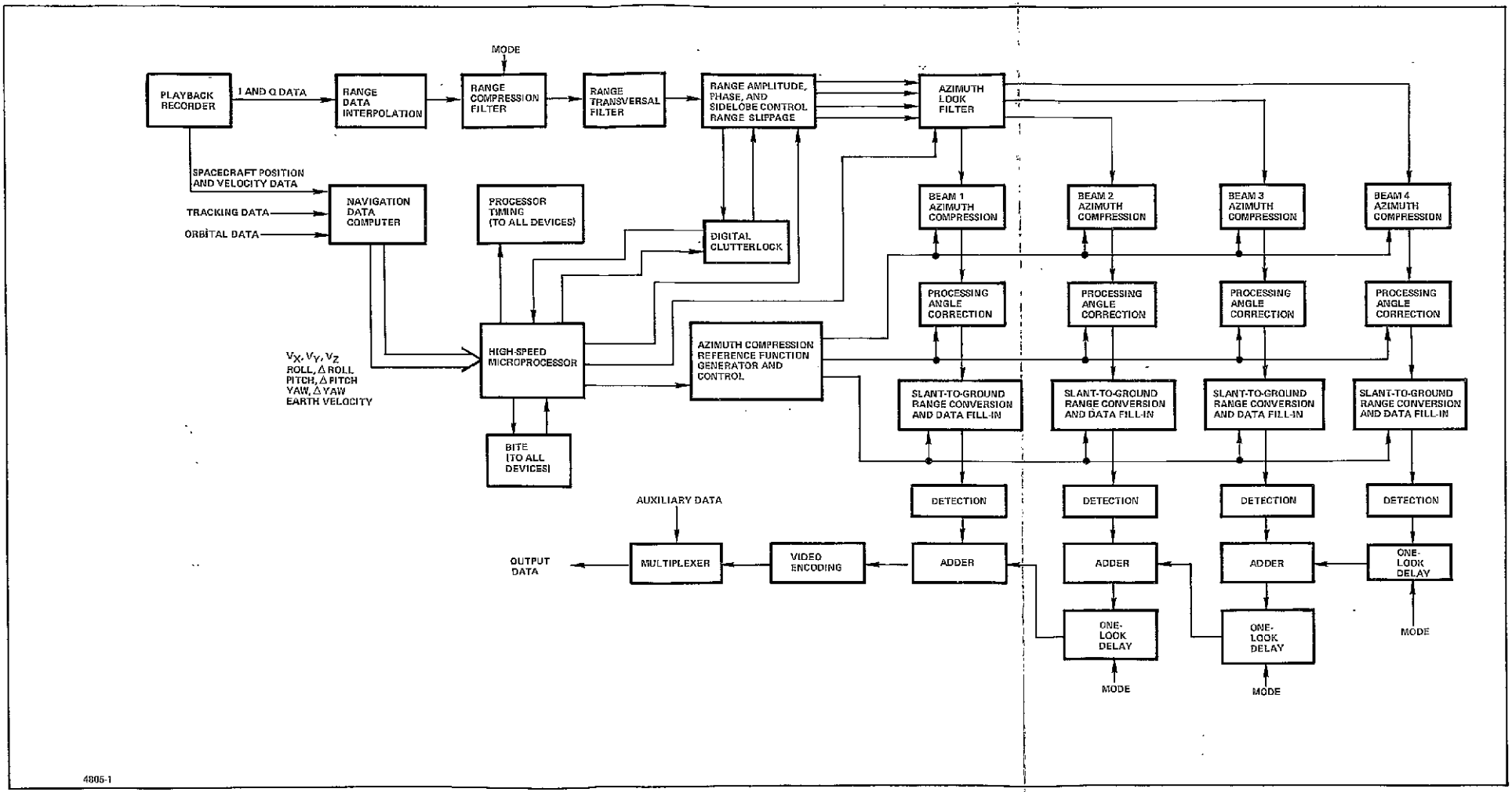


Figure 10 - Space Shuttle SAR Processor Block Diagram

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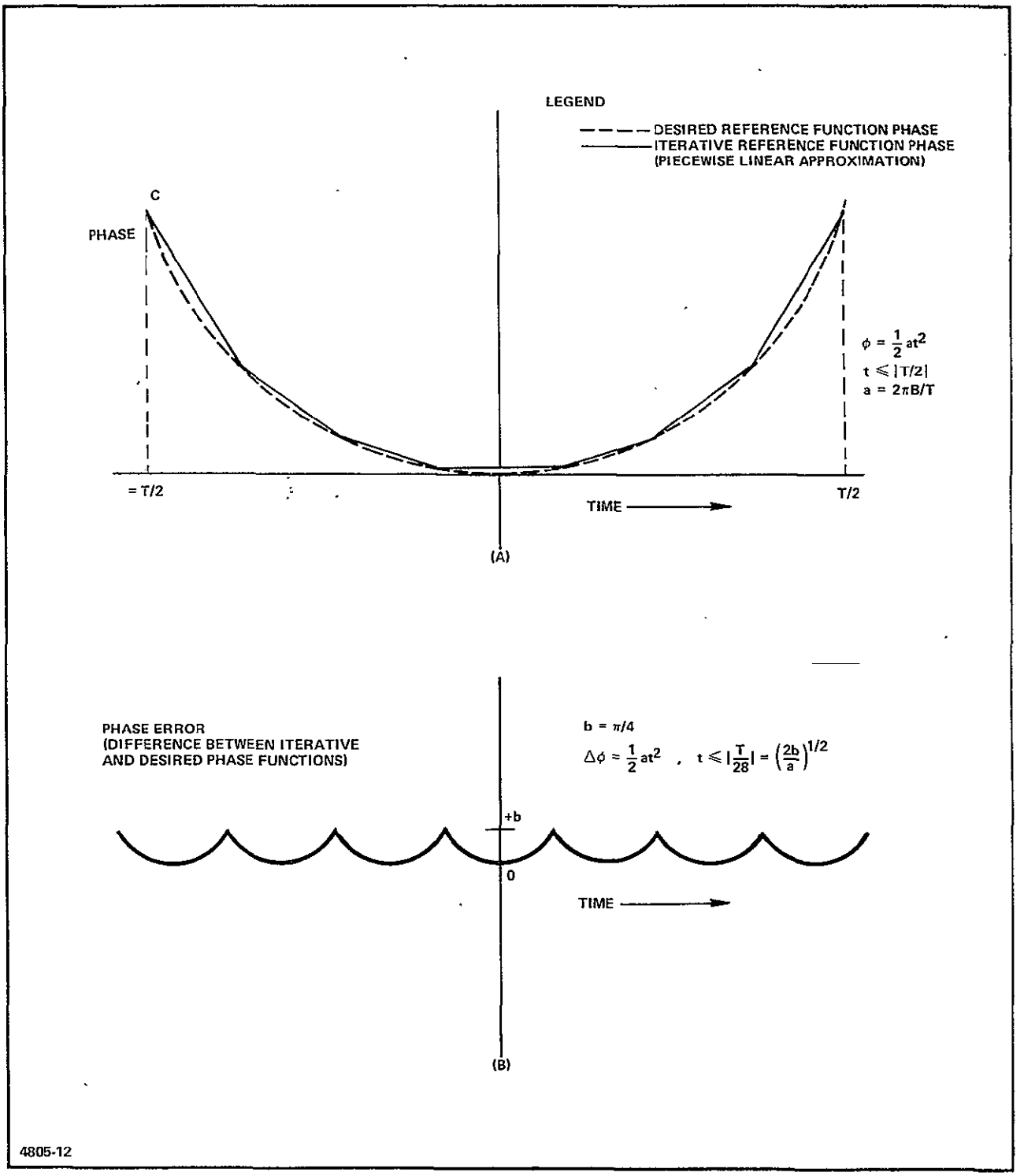

Figure 11- Reference Function for an Iterative Range Compression Filter

It is estimated that the RCF will require 30 printed circuit boards, utilize 2250 integrated circuits, and consume 750 watts.

3. RANGE AMPLITUDE, PHASE, AND SIDELOBE CONTROL FILTER

This unit is essentially a very high-speed array of complex multipliers, storage, and read only memories (ROM's). Its purposes include:

1. Weighting of the range compressed signal for sidelobe control
2. Adjustment of amplitude across the range swath for antenna elevation pointing angle correction
3. Application of the required phase correction to each range cell as dictated by the clutterlock and navigation computer
4. Performance of range slippage
5. Offsetting the azimuth spectrum for azimuth look filtering
6. Reduction of the range dimension sampling rate (if increased in the range compression filtering).

The complexity of the algorithm used for range sidelobe control will be dictated by the peak and integrated sidelobe specifications.

Fine range slippage requires a range dimension interpolation. It is performed by storing samples of the weighting function spaced at much finer intervals than the data samples. Then, as illustrated in Figure 12, the center of the stored function is aligned with the point at which a data point is to be reconstructed, and reference function points are accessed from addresses corresponding to existing data. A digital convolution is performed, resulting in the interpolated data point.

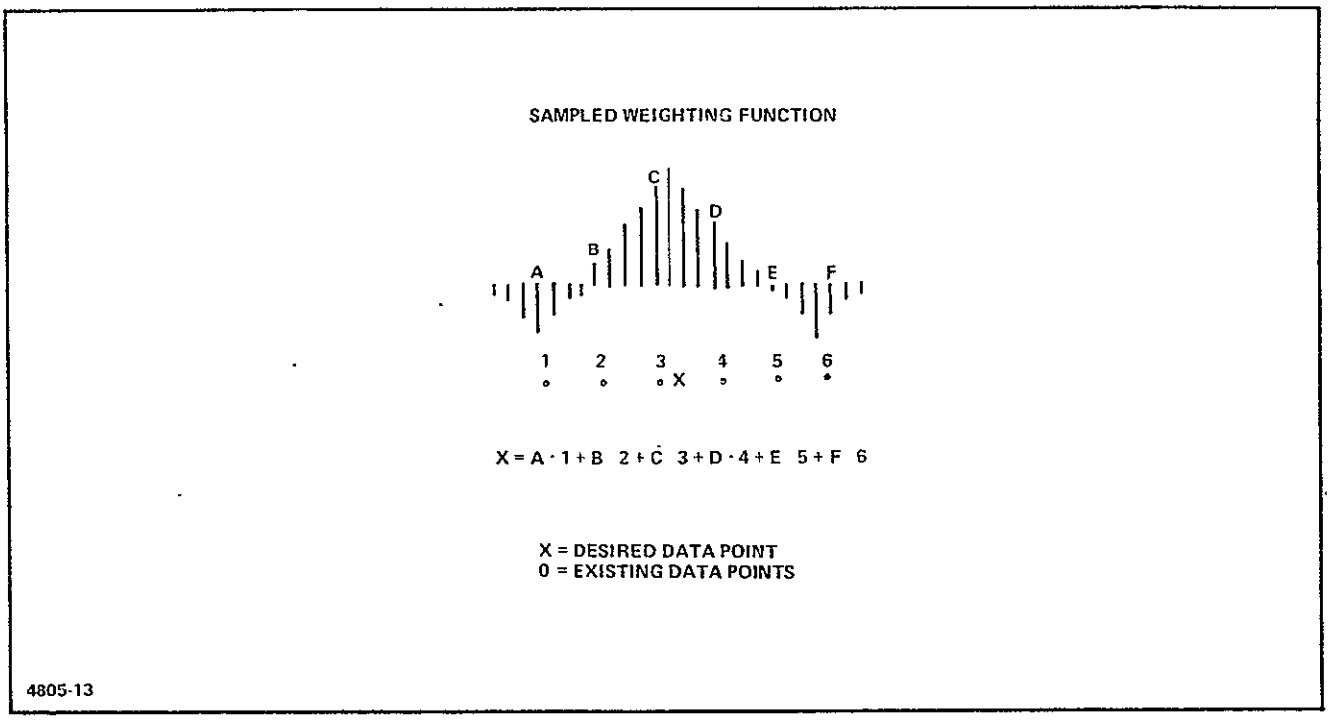

Figure 12 - Digital Interpolation

Offsetting the spectrum in azimuth is a phase adjustment, i.e., a vector rotation. One complex multiplication per output data point is necessary to perform this task. The azimuth offset operation allows all four azimuth looks to be formed by low-pass filtering operations by translating the desired center frequency of each azimuth look to zero. A generalized block diagram is shown in Figure 13.

It is estimated that the range amplitude, phase, and sidelobe control filter will require 10 boards, 600 integrated circuits, and consume 300 watts.

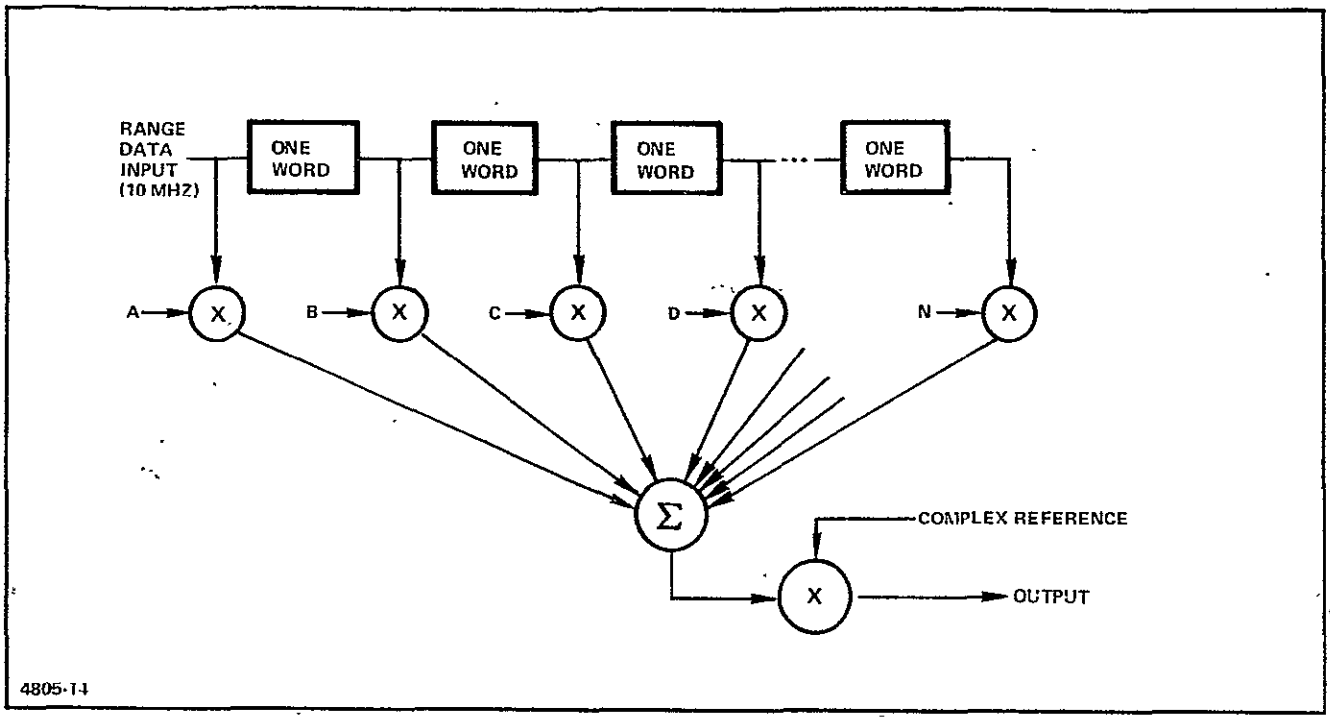

Figure 13 - Range Filter Block Diagram

4. AZIMUTH PREFILTER

The azimuth prefilter consists of a bank of four nonrecursive low-pass filters, each filter separating, shaping, and weighting the spectrum for one of the azimuth looks. The data rate will be reduced to the minimum (approximately one complex sample for every 20 meters of spacecraft travel) at the filter output to maintain the minimum azimuth compression filter memory size. In addition to the filtering, coarse range slippage (i.e., integer range gate slippage) is also performed in this unit.

The azimuth prefilter will be implemented with "integrate and dump" filter sections. This type of filter, illustrated in Figure 14, digitally convolves N contiguous data points with an N-point low-pass filter function and outputs one data point. Therefore, if the input data rate is sampled at the Nyquist rate, and if the bandwidth is to be decreased by a factor of four, then N/4 sections must be time-multiplexed to maintain an adequate sampling rate.

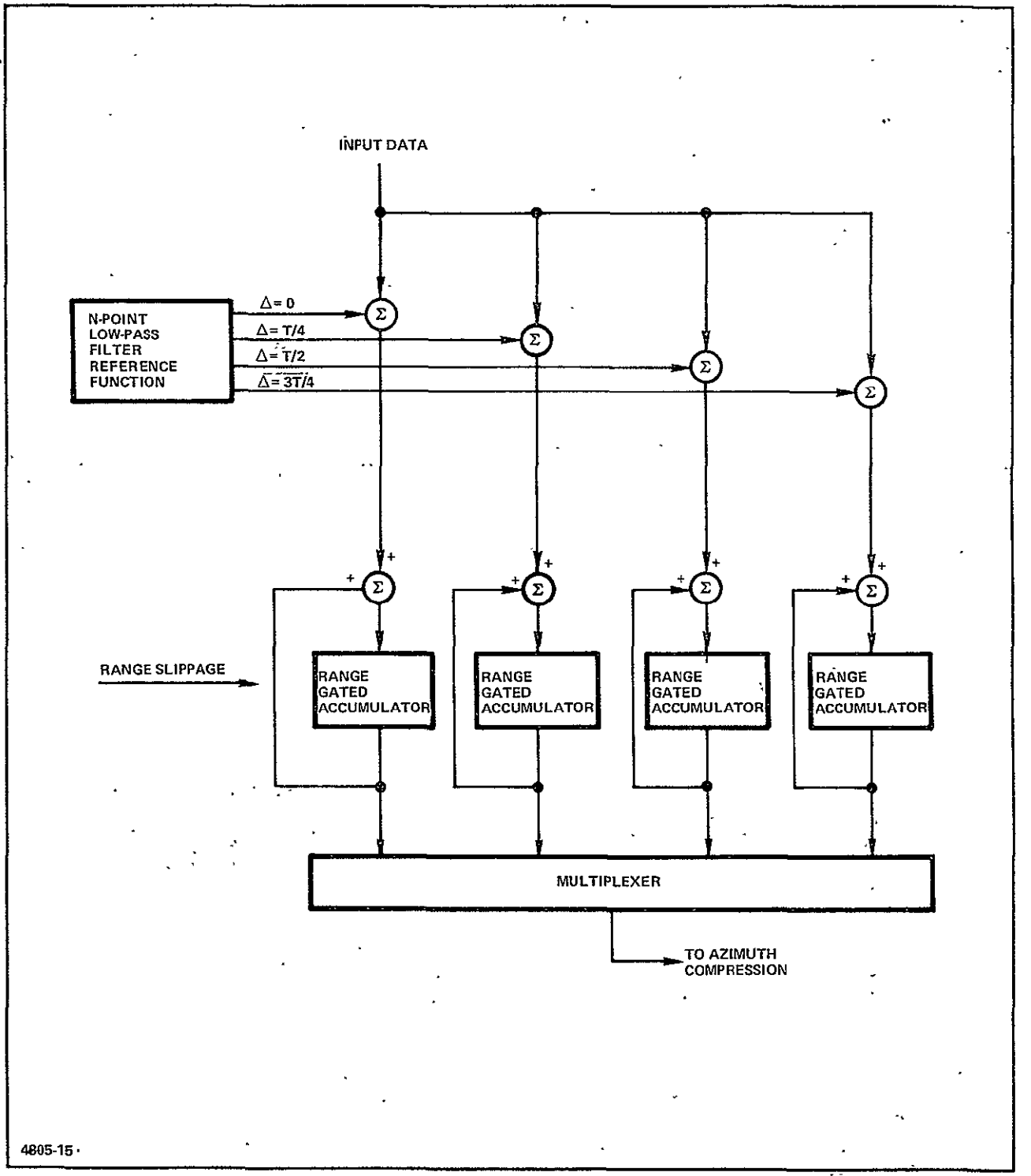

Figure 14 - Azimuth Prefilter (One of Four Sections)

Every data point entering a filter section is multiplied by N/4 evenly spaced samples of the low-pass function, and each product is added to the sum stored in one of the N/4 accumulators. After N products have been summed in any accumulator, its contents are dumped, it is cleared, and a new convolution is initiated. Thus, for every N azimuth sample input, the contents of each accumulator is dumped once.

To obtain the required sidelobe levels after azimuth compression, the filter will include a weighting function, as was done in the range dimension. Because pulse weighting and pulse compression are linear operations, weighting may be performed prior to collapsing with no detrimental effects. (In fact, weighting of the low-pass filter reference function actually reduces the complexity of the design of this device, because passband droop is now a desirable feature.)

The azimuth prefilter reference function will have only an in-phase component. Any operations requiring complex multiplications to implement will be done in the azimuth compression filter. This will simplify the arithmetic in the unit, both for the generation of the filter function, and for the hardware required to perform the convolution.

The value of N required for the azimuth prefilter will be determined by the processor integrated sidelobe specifications. Because the output data rate is being reduced by a factor of four, the power in the filter's stop band will lay over its passband threefold. Thus, a sharp transition band and low passband ripple are very desirable. Four filter sections have been assumed for this estimate, allowing for the use of a 16-point reference function.

The azimuth prefilter must handle data at the same rate as all devices preceding it, because the rate is not reduced until the data are output. Therefore, 10-MHz operation is necessary. This unit is estimated to require 30 boards with 1600 integrated circuits, and will require 750 watts.

5. AZIMUTH COMPRESSION FILTER

The azimuth compression filter (ACF) is the largest unit within the digital signal processor. It consists of an input data buffer, the 22.1 megabit azimuth compression memory, the azimuth compression reference function generator, 344 complex multipliers, four 86-point summing networks, range and azimuth interpolation networks which produce ground range samples spaced by 12.5 meters and align the azimuth looks for addition, and detectors. Each ACF section compresses data by convolving them with the proper matched filter reference function, as illustrated in Figure 15. After each compression, the data are shifted by one position, a new range sweep is entered, and the process is repeated.

In addition to the parabolic phase function necessary to compress the azimuth phase history for each of the looks, the reference function used in the ACF must account for such factors as the antenna beam shape (including such factors as those introduced by spacecraft pitch), any further weighting required for sidelobe control, changes in the ground sample positions (caused by acceleration, earth rotation, etc.), and antenna slewing. The ability of the convolution processor to continually modify the ACF reference function to optimize the processing is a major advantage of this algorithm.

The ACF reference function is complex; i.e., it has an in-phase and quadrature component. It can be expressed as

$$h(X) = f(X)\, e^{j\Phi(X)} = f(X)\left[\cos\Phi(X) + j\sin\Phi(X)\right] \quad , \qquad (13)$$

where

$h(X)$ = the complex reference function

$f(X)$ = an amplitude shaping function

$\Phi(X)$ = a real phase function

X = the azimuth coordinate

and $j = (-1)^{1/2}$.

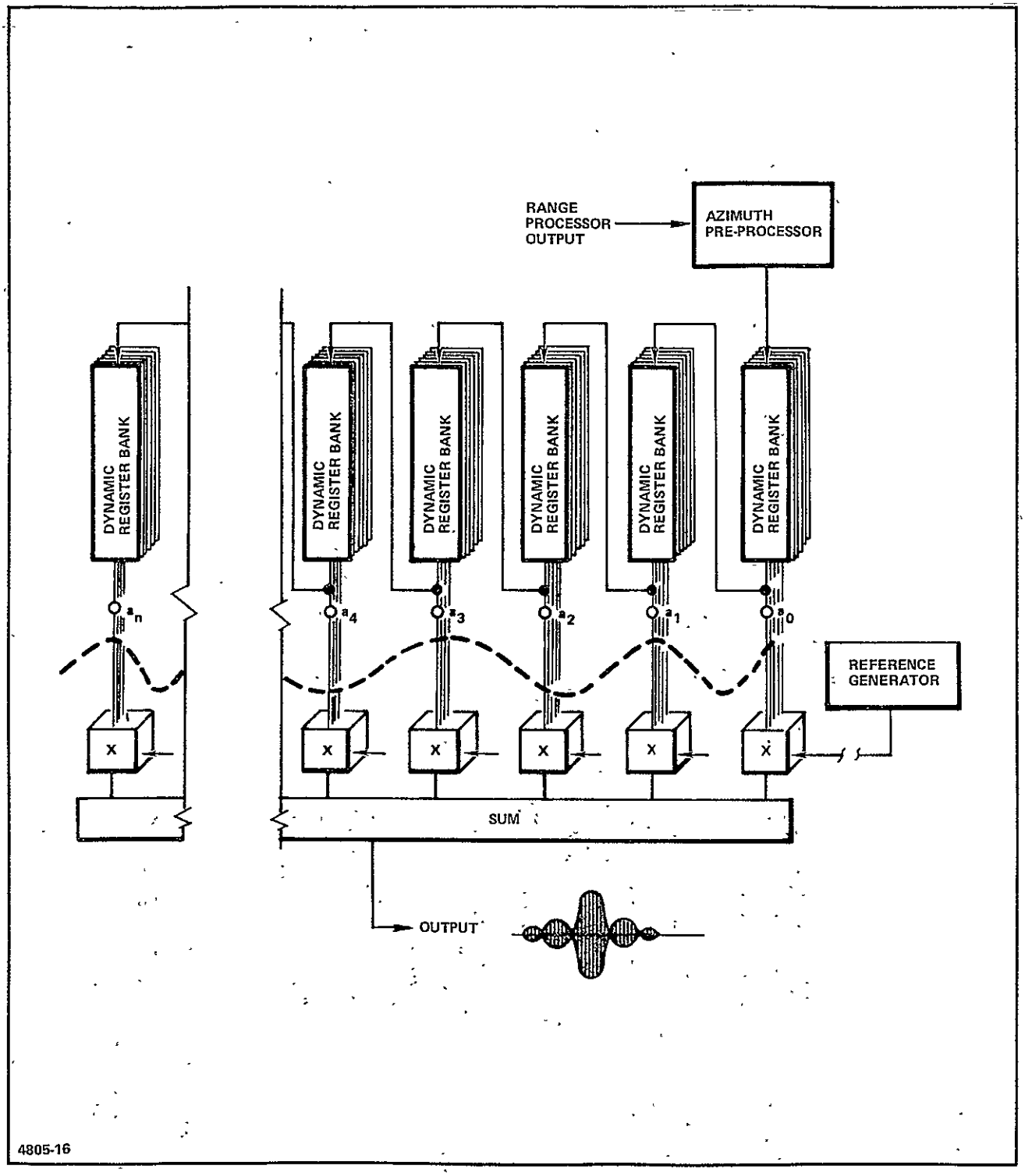

Figure 15 - SAR Processor Using the Convolution Algorithm

For the geometry illustrated in Figure 16, the phase term in the reference function is given by

$$\Phi(X) = \frac{4\pi}{\lambda} R(X)$$

$$= \frac{4\pi}{\lambda} R_o + \cos \psi_o X + \left[\frac{\sin^2 \psi_o}{2R_o}\right] X^2 + \left[\frac{\cos \psi_o \sin^2 \psi_o}{2R_o^2}\right] X^3 \ldots , \quad (14)$$

where

$R(X)$ = the slant range to the target

R_o = the slant range to the center of the synthetic aperture

ψ_o = the yaw angle plus the squint angle of the look.

The constant term can be ignored. The linear term in X, which does not depend on range, is corrected for in the range filtering. The cubic term is orders of magnitude smaller than the squared term and can be neglected. The phase function therefore becomes

$$\Phi(X) = \frac{2\pi R_o}{\lambda}\left(\frac{X \sin \psi_o}{R_o}\right)^2 . \quad (15)$$

The number of range cells for which this phase function may be used was analyzed in Section II, paragraph 5.

Upon completion of the azimuth compression, a two-dimensional interpolation must be performed. This interpolation will

1. Generate data points spaced by 12.5 meters in both range and azimuth
2. Remove the squint angle from the four azimuth looks for proper addition.

Figure 17 illustrates this process.

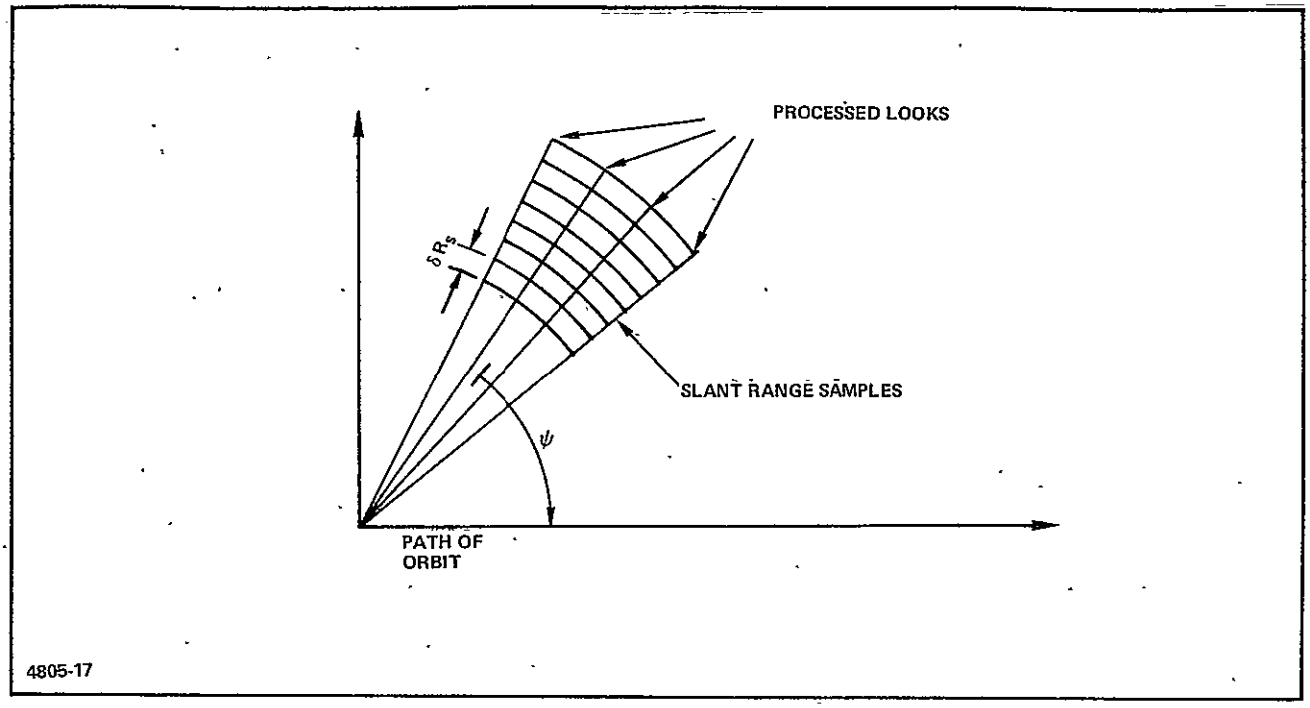

Figure 16 - Phase Term in Reference Function

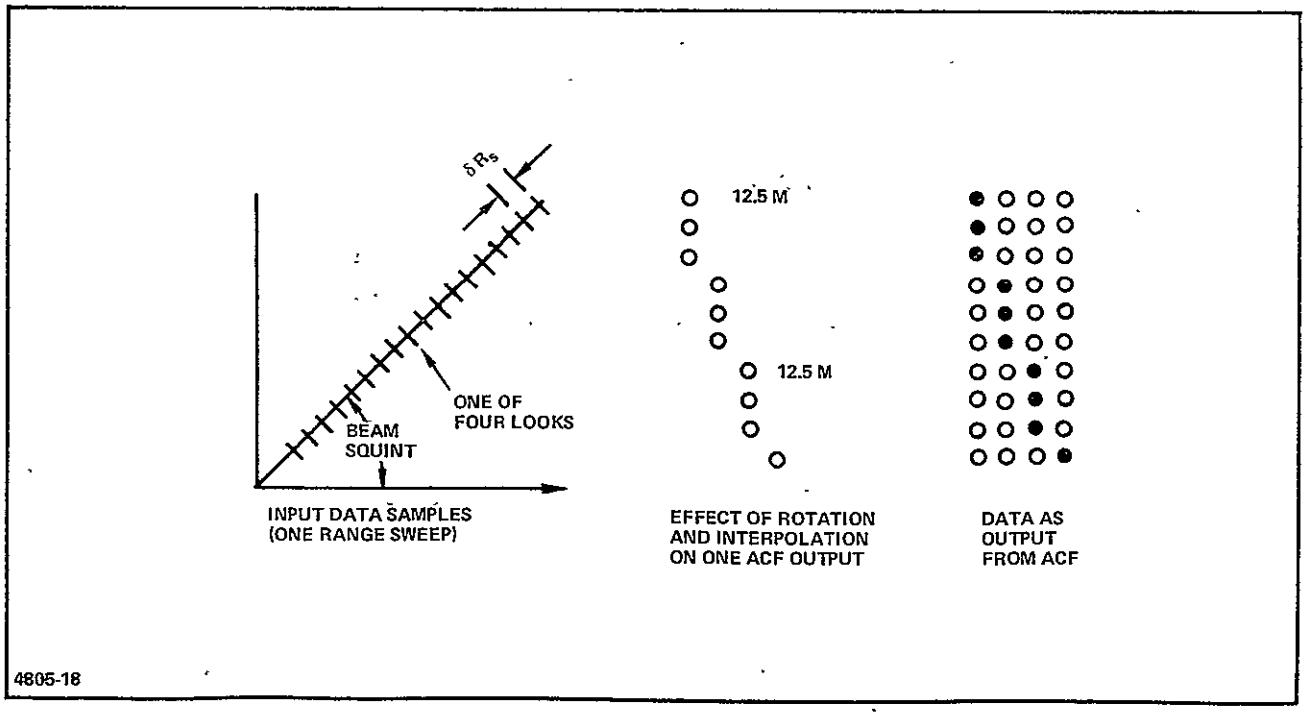

Figure 17 - Postcompression Coordinate Transformation

The slant-to-ground range conversion process was described in Section II, paragraph 6. The azimuth interpolation is a similar process in an orthogonal coordinate, although the azimuth resampling does not change the sample spacing (the sample spacing interpolation is performed in the azimuth compression filter), but only removes the processing angle.

At the completion of the interpolation processes, the signals will be detected typically by forming $(I^2 + Q^2)^{1/2}$. After azimuth look summation, the data will be encoded.

The ACF described in this section is estimated to require 180 boards. It will require 9250 integrated circuits, assuming 1350 charge-coupled devices (CCD's) (16,384-bit memories) will form the bulk storage illustrated in Figure 15. The unit is estimated to require 4350 watts.

6. AZIMUTH LOOK SUMMATION

As was described in Section II, paragraph 1, a 22-megabit cache storage is required for retaining looks until corresponding data points are available for addition. This memory required a 33.7-megabit per second access rate (9-bit words) for real-time operation. Considering the size, speed, and mode dependence of the memory accessing, a solid-state storage has been sized for the digital signal processor.

This memory has been estimated using a 64k-bit CCD, projected to be available within three years (see Section V, paragraph 1). The storage would require 336 of these devices.

The azimuth look summation circuitry is estimated to require 10 circuit boards, contain 400 integrated circuits, and consume 400 watts.

7. DIGITAL CLUTTERLOCK

Figure 18 is the basic block diagram for the proposed digital clutterlock. ROM's will be used to determine the magnitude and phase of each range compressed data point. The change in phase from sample to sample for a particular range, $\Delta\phi$, is determined by

subtraction. Next, $\Delta\phi$ is compared with the average phase change for a given range, $\overline{\Delta\phi}$, to determine the rate of change of the phase. (A constant rate of change would imply the antenna is not slewing in azimuth.) The difference in the sample value and the average value are accumulated, this process effectively filtering statistical noise. Overflow of the accumulator (either positive or negative) will cause $\overline{\Delta\phi}$ to be modified. The loop time constant will be on the order of the travel time across a small number of null-to-null azimuth beamwidths.

The amplitude circuitry serves to warn the clutterlock that the data are being received from a low return area or radar shadow and may not have sufficient signal-to-noise, or that a land-water boundary has been crossed and rapid phase change will be expected.

The range gated $\overline{\Delta\phi}$ and $\bar{A}$ estimates will be used to generate a "best fit" curve. The allowable curves are generated by computation of the zero frequency paths for the possible antenna ambiguities and rotations, as explained in Section II, paragraph 2. This information is used to track the antenna ambiguity and antenna rotation during the processing and to generate the required azimuth phase and amplitude correction signals. The information may also be stored to aid in processing of other polarizations or frequencies.

The digital clutterlock will receive computational assistance from the microprocessor and a general-purpose minicomputer. It is estimated to require 10 boards, 600 integrated circuits, and consume 200 watts.

8. PROCESSOR COMPUTATION AND CONTROL DEVICES

A high-speed microprocessor is used to control the digital signal processor. It is used to generate filter reference function coefficients and perform other varied computations which must be made periodically, as well as interface the digital signal processor with external equipment. It is estimated that the microprocessor required for this application will require 10 circuit boards, 600 integrated circuits, and consume 250 watts.

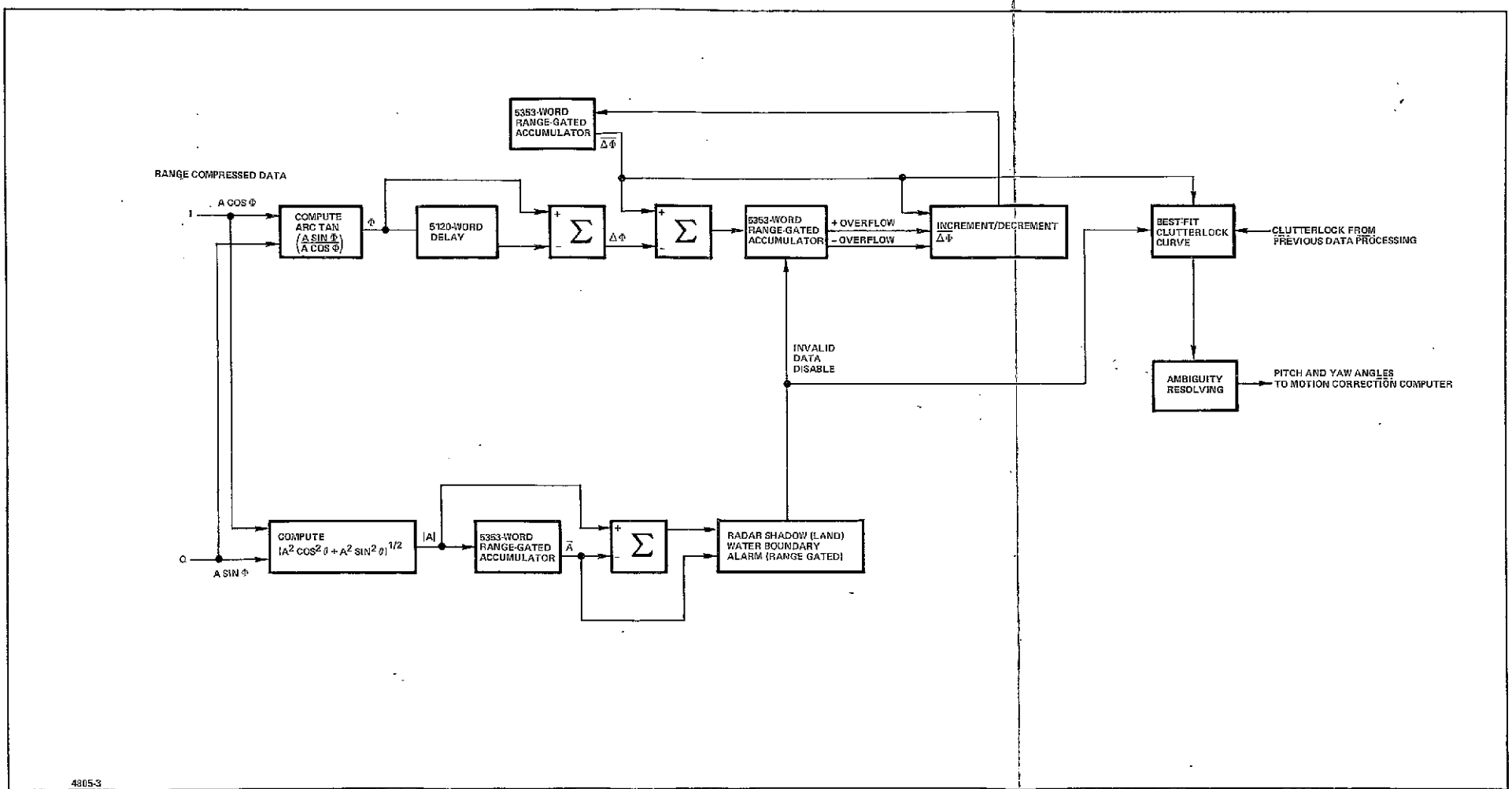

Figure 18 - Digital Phase Clutterlock

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An associated minicomputer will serve a variety of purposes from generation of test signals while off-line to performing calculations involving spacecraft position, velocity, acceleration, and attitude while on-line. It should be able to utilize information from the data tapes as well as data from ground-based tracking stations, thus interfacing the processor with auxiliary data devices.

Any of a host of commercially available small computers are available for this task. The specifics of the machine depend much upon the various uses for which it is intended (especially when off-line). Typically, such a machine requires 1500 watts.

9. BUILT-IN TEST EQUIPMENT (BITE)

For a digital signal processor of this magnitude, rapid fault isolation is imperative. A testing philosophy which processes radar data in multiple locations while the processor is on-line and comparing the processed outputs has proven to be an excellent method of accomplishing this task. A well-designed BITE system, using the concept, will isolate a fault to a replaceable unit, which may be replaced immediately and repaired when time permits.

The BITE will make extensive use of integrated circuit microprocessors, utilizing their inherent power to perform calculations identical to those performed by the processor (but at a reduced rate of speed and with a greatly reduced number of integrated circuits) and to compare the results with sampled processor values.

For this processor, it is estimated that the BITE will require 20 circuit boards, 1200 integrated circuits, and consume 450 watts.

10. SUMMARY OF PROCESSOR COMPONENTS

Processor components in the space shuttle radar are summarized below:

Unit	No. of boards	No. of IC's	Power
Range compression filter	30	2,250	750
Range amplitude, phase and sidelobe control	10	600	300
Azimuth prefilter	30	1,600	750
Azimuth compression filter	180	9,250	4,350
Azimuth look summation	10	400	400
Digital clutterlock	10	600	200
Microprocessor	10	600	250
BITE	20	1,200	450
General-purpose minicomputer	-	-	1,500
Total	300	16,500	8,950.

It is estimated that the processing system and all peripheral equipment will be packaged in three racks, sized 6-1/2 feet by 2-1/2 feet by 2 feet, and have a total weight of 3000 pounds.

The processor estimate has been based on previously described CCD memory devices and predominantly Schottky logic, with a reduced size and power consumption factor based on anticipated advances in LSI devices described in Section V.

11. PROCESSOR GROWTH

The processor described in Section IV could be used with minor modifications (primarily time constants) to process data from 278- and 370-km orbits. The four-look operation would be retained, and the resulting azimuth resolutions would be 30.65 and 35.36 meters for the respective orbits. Maintaining 25-meter resolution with fewer looks would be possible, but the modification is more complex.

If 25-meter resolution is to be maintained, the size of the ACF and azimuth look summation networks will increase linearly with range. Thus, for operation at 370-km altitude, it is anticipated that an additional 190 circuit boards will be necessary, thereby increasing the processor size by over 60 percent.

SECTION V - TECHNOLOGY SURVEY

1. GENERAL

A portion of this program was spent examining new memory and logic technologies which may influence the processor design. Emphasis was placed upon determining the advancements which had a high probability of resulting in major new products available within the next three years. In this section, the results of the technology survey will be presented. Table IV lists the names and addresses of individuals contacted.

2. MEMORY TECHNOLOGY

The most promising technology for producing large memory devices with high data rates is the CCD. This technology should be used to mass produce memory devices of 16k bits and larger, having data rate of 10 MHz, and dissipating a mere 10 μW per bit within the next year. The per-bit price for commercial devices has been projected to be less than one-tenth cent per bit in three to five years.

Digital CCD's having 16,384 bits have recently been announced by Intel, Fairchild, and Bell-Northern. Intel's device is constructed as 64 parallel, 256-bit multiplexed shift registers with single data input and data output pins. It requires four phased clock signals. The read/modify/write cycle time is 620 ns. The Fairchild device is organized as four parallel 4096-bit devices, each composed of 32 parallel 128-bit multiplexed shift registers. Each section has a read/modify/write cycle time of 300 ns. The device only requires one clock. The Bell-Northern device is organized as four parallel 4096-bit shift registers. It requires two phased clocks. The Northern-Bell device is in a 16-pin package, Intel in an 18-pin package, and Fairchild a 24-pin package. The Fairchild and Bell-Northern devices would be preferable for the proposed processor.

TABLE IV - CONTACTS WITH SEMICONDUCTOR MANUFACTURERS AND CONTRACTORS

Organization	Name	Technology	Address/phone
Texas Instruments	Richard Horton	I^2L	713-494-5115
	Jerald McGee	I^2L	713-494-5115
Motorola	James Bunkley	I^2L	602-244-3714
	Robert Jenkins	EFL	602-962-3346
TRW	Barry Dunbridge	EFL	TRW Systems Group, One Space Park, Redondo Beach, CA 90278
RCA	Albert Sheng	I^2L/SOS	201-722-3200 (2612)
	Raymond Minet	CCD	717-397-7661 (2294)
	Michael Diagostino	SOS	201-722-3200 (2507)
Fairchild	Frank Bower	CCD	415-493-7250 or 8001
Intel	Kenneth Kwong	CCD	408-246-7501
	Donald Bryson	CCD	408-246-7501
Air Force Avionics Laboratory	Ronald Belt	CCD	513-255-2459
	Millard Mier	Magnetic Bubbles	513-255-2459
	Stewart Cummins	Magnetic Bubbles	513-255-2459
Bell-Northern Research	William Coderre	CCD/SOS	613-596-4439, Manager, Technology Liaison, Dept. 5G20, Bell-Northern Research, P.O. Box 3511, Station C, Ottawa, Canada KIY487

It should be emphasized, however, that CCD development is oriented toward the computer industry, and that CCD's will require operating conditions with temperatures below 70 deg C. Thus, for a ground station processor, they appear to be an excellent memory device, but for spacecraft operation, both component qualification and careful thermal design will be necessary, both of which could prove extremely expensive.

Conventional MOS technology appears to be rushing to meet the challenge of CCD's. The announcement of a 16,384-bit MOS random access memory (RAM) was hinted at by several manufacturers, but a formal announcement will probably not be made during 1975. Prices of these devices have been projected to be competitive with CCD's.

Magnetic bubble technology was discussed with the Air Force Avionics Laboratory. This technology does not appear imminent enough for the proposed processor timetable.

Integrated injection logic (I^2L) is a bipolar technology which may also be a viable alternative within the next few years. A 4096-bit RAM using this technology is anticipated by the end of this year, and much larger devices are projected. I^2L has very high packing densities, requires relatively low power, and has a -55-degree to +125-degree Celsius temperature range.

3. LOGIC TECHNOLOGIES

During the next three to five years, small, medium, and large scale integration (SSI, MSI, and LSI) high-speed logic families will probably continue to utilize Schottky and low-power Schottky TTL and ECL. These logic families are very large, readily available, familiar to designers, and have reached near minimum cost. Although new devices will be emerging, they will probably be improvements on and extensions of existing logic families.

Three new technologies which are being heralded for very large scale integration devices are integrated injection logic (I^2L), emitter follower logic (EFL), and silicon-on-sapphire CMOS (SOS). Texas Instruments appears to have the largest I^2L development program.

A four-bit microprocessing element, the SBP0400, has already been introduced, and the company projects a full line of computer products within three years. Among the advantages of I^2L technology are extremely high packing density (a factor of 10 above TTL), static operation, TTL compatibility, a -55-deg to +125-deg C temperature range, and a virtually constant propagation power product.

The SOS technology is being most strongly pursued by RCA. A large number of LSI devices are also projected for introduction within a year. If successfully produced, SOS CMOS circuits promise Schottky TTL speeds with one to two order of magnitudes less power consumption. The SOS technology should be faster because of the lower parasitic capacitance of the sapphire substrate and have higher densities than conventional CMOS by at least a factor of two.

The major obstacle to SOS technology appears to be the cost of the sapphire substrate, which presently is 10 times that of conventional silicon. RCA feels, however, that eventual demand for these devices will greatly lower production costs, making them competitive with conventional CMOS.

The EFL technology has been referred to as a "Cinderella" and a "sleeper." This pre-TTL configuration is being studied by such companies as TRW and Motorola. EFL circuits have the same cell size as I^2L but promise much higher speeds. EFL may be the longest in development of these technologies, because Motorola says no marketable products are presently in development, and TRW has produced only customized devices.

SECTION VI - PROCESSOR COSTING AND SCHEDULING

1. GENERAL

Paragraph 2 of this section presents costing of the design and development of a ground-based processor described in Section IV in terms of man-hours and material dollars and a program schedule (two years) over which the program would last. Paragraph 3 discusses factors which must be considered if a spaceborne processor is to be constructed.

2. GROUND-BASED PROCESSOR

Table V lists costs of developing a ground-based processor system. Figure 19 is the program schedule. A manloading estimate for this program is shown at the bottom of the figure. This processor has been costed on the basis of a laboratory environment, the use of commercial grade components, and commercial design and development practices. The playback recorder has not been included in the cost estimate.

3. SPACEBORNE PROCESSING SYSTEM

Costing and scheduling of the development of a spaceborne processing system is extremely speculative with the information available at this time. When the design parameters become better defined, it is felt that these numbers may be factored into the data presented in Table V to estimate the actual cost.

Discussions with engineers involved in the development of previous spacecraft systems have tended to project a three-year development program is possible (although a highly coordinated effort is required). This estimate is speculative as many parameters affecting the program are not defined.

TABLE V - GROUND-BASED PROCESSOR COSTING

Item	Hours (senior)	Hours (junior)	Computer	Material (dollars)
Program administration	7,000	7,000	200	
Systems studies	6,000	1,500	200	
Design and development	8,500	31,000	500	100,000
System fabrication	7,000	41,000	50	200,000
System integration and testing	3,000	6,000	50	
Acceptance testing	400	800		
Documentation	4,000	8,500		
Installation and checkout	100	500		
Operation and maintenance training	500	500		
Total	36,500	96,800	1,000	300,000

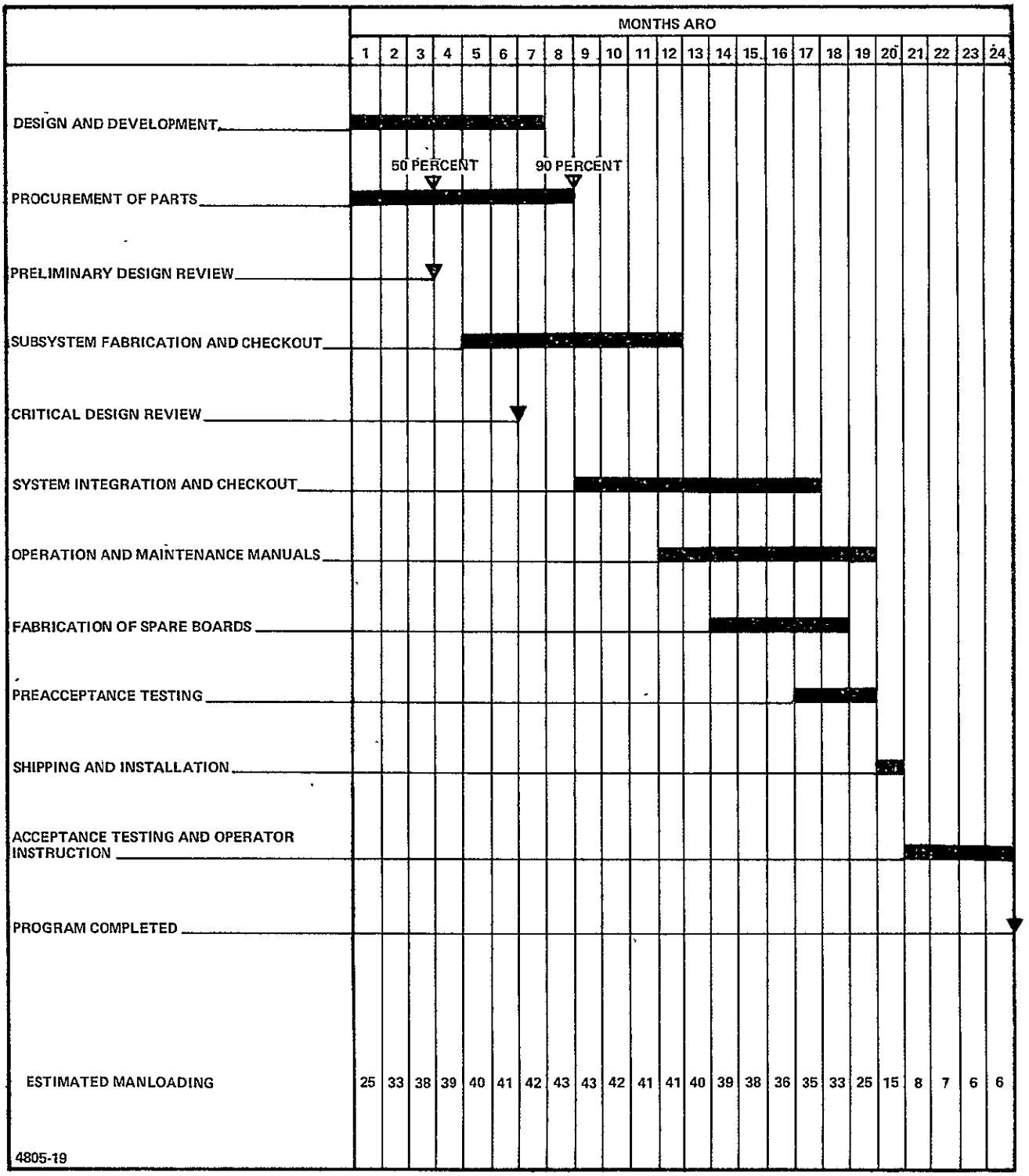

Figure 19 - Space Shuttle SAR Digital Signal Processor Development Schedule (Ground-Based Processor)

Thus, although a spaceborne processing system could most certainly be developed, its extended program time and much higher cost must be carefully weighed against the benefits it could produce.

SECTION VII - CONCLUSIONS

A digital signal processor for producing imagery made from a spaceborne radar operating at L- and X-band is indeed feasible. Indeed, more complex processors than this are presently being built. The processor may be deployed either as a ground-based system, fed by tape recorded and/or data linked data, or as a piece of equipment in the manned laboratory area of the shuttle.

The increased cost of a spaceborne processor plus the increased development time (based on experience with previous spaceborne hardware) weigh heavily against this option. Unless real-time operation for any possible orbit (i.e., the need for processing data exists when a data link to a ground-based processor is not available) is absolutely necessary, the cost effectiveness of this option seems very low.

The technology to build this processor exists today. Future advances in memory and LSI will be able to reduce its size, cost, power consumption, etc., but as the complete capability of the radar is being utilized, no improvement in performance will result.